PhD Research Article / Doktora Çalışması Araştırma Makalesi

LOW VOLTAGE LOW POWER NEURON CIRCUIT DESIGN BASED ON SUBTHRESHOLD FGMOS TRANSISTORS

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ABSTRACT

In this work, design of low-voltage low-power analog artificial neural network (ANN) circuit blocks by using subthreshold floating-gate MOS (FGMOS) transistors and a neuron circuit is implemented. The circuit blocks, four-quadrant analog current multiplier and FGMOS based differential pair, have been designed and simulated in CADENCE environment with TSMC 0.35µm process parameters.

Keywords: Neuron circuits, subthreshold, FGMOS transistors, low voltage, low power, neural network, hardware implementations.

EŞİKALTI FGMOS TRANSİSTORLAR KULLANILARAK DÜŞÜK GERİLİM VE DÜŞÜK GÜÇTE ÇALIŞAN NÖRON DEVRESİ TASARIMI

ÖZET

Bu çalışmada, eşikaltı bölgesinde çalışan yüzer geçitli MOS (FGMOS) transistorlar kullanılmasıyla düşük gerilimde çalışan ve az güç tüketen analog yapay sinir ağı (YSA) devre bloklarının tasarımı yapılmış ve bir nöron devresi gerçeklenmiştir. Dört bölgeli akım çarpıcı ve FGMOS tabanlı farksal çift devreleri TSMC 0.35µm proses parametreleri kullanılarak CADENCE programında tasarlanmış ve benzetimi yapılmıştır.

Anahtar Sözcükler: Nöron devresi, eşikaltı, FGMOS transistor, düşük gerilim, düşük güç, yapay sinir ağı, donanım gerçeklemeleri.

1. INTRODUCTION

Artificial Neural Networks (ANNs) have been widely used in many fields. A great variety of problems can be solved with ANNs in the areas of pattern recognition, classification, signal processing, control systems etc. Most of the work done in this field until now consists of software simulations, investigating capabilities of ANN models or new algorithms. However, hardware implementations are also essential for applicability and for taking the advantage of neural network's inherent parallelism. Neural network hardware implementations are important to realize any required function. Nowadays, one of the greatest aim of microelectronics science is to

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develop a general purpose integrated circuit which can change own characteristics or transfer functions with respect to any condition. Neural integrated circuits are this kind of proposed circuits with on chip or off chip learning capabilities.

Low power consumption design techniques have become more and more important in modern VLSI technologies. This has been mainly motivated by the demand for portable equipments which must consume as little power as possible to extend the battery life. Weak inversion mode is suitable for the design of continuous time ultra low power systems [1].

FGMOS structures are also known as neuron MOS because of functional similarity of the neuron [2]. FGMOS transistors biased in the weak inversion region exhibit an exponential behavior which can be used to implement various current mode circuit such as multipliers and dividers [3]. In the last few years, FGMOS transistors have found many applications in electronic programming [4], Op-amp offset compensation [5], D/A and A/D converters [6], inverters and amplifiers [7], voltage attenuators [8], current mirrors [9] and low voltage analog circuits [9]-[11]. Recently, an increased number of publications on the use of the FGMOS in analog computational circuits have been reported voltage squarers and multipliers [11]-[13].

In previous studies, the neuron circuit generally has the following components; current mode multiplier, an Op-amp based adder and activation function generator [13]. The summation and the activation function were realized in different blocks. In this paper unlike the previous works, these functions were realized in the same subthreshold FGMOS differential pair block.

In this work, using subthreshold FGMOS based multiplier and subthreshold FGMOS differential pair, a neuron was designed. Then, n-input neurons are obtained by generalized this neuron structures. Finally the designed low voltage low power subthreshold FGMOS based neuron circuit was simulated in CADENCE environment with TSMC 0.35μm process parameters. All simulation results were shown and concluded.

2. SUBTHRESHOLD FGMOS TRANSISTOR

The multiple-input-floating-gate transistor is an ordinary MOS transistor which the gate is floating. The basic structure of an n-channel FGMOS transistor with n-input voltages V_1, V_2, . . ., V_n, is shown in Figure 1. The floating-gate is formed by the first polysilicon layer over the n-channel while the multiple-input gates are formed by the second polysilicon layer and they are located over the floating gate. This floating gate is capacitively coupled to the multiple-input gates. The symbolic representation of such devices is shown in Figure 1.
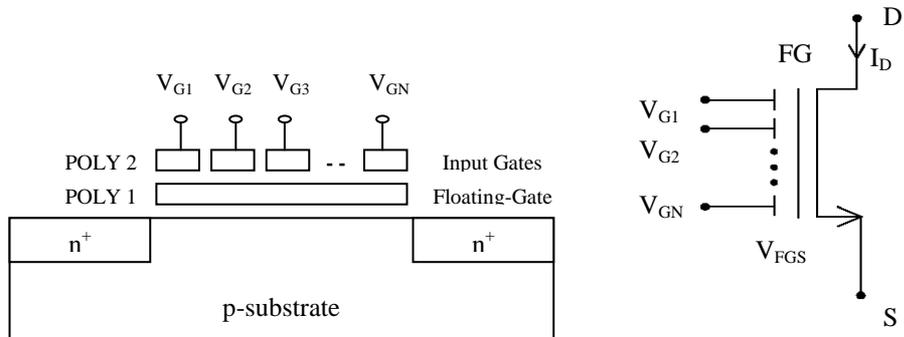

Figure 1. Basic structure of an NMOS floating-gate transistor with n input gates and symbolic representation.

The drain current of a an n-channel FGMOS transistor with n-input gates in the subthreshold saturation region, neglecting the second-order effects, is given by the following

equation ($V_{GS} < V_T$, $V_{BS} = 0$, $V_{DS} > 4U_T$):

$$I_D = I_0 e^{\frac{V_{FGS}}{nU_T}} \tag{1}$$

where I_0 is the weak inversion specific current, n is the slope factor and U_T is the thermal voltage.

The voltage at the floating gate (FG) is given by:

$$V_{FG} = \frac{C_{FGD}V_D + C_{FGS}V_S + C_{FGB}V_B + \sum C_{Gi}V_{Gi}}{C_T} \tag{2}$$

where V_{FG}, V_D, V_S and V_B are the voltages at the FG, drain, source and bulk respectively; N is the number of inputs; C_i are their corresponding input capacitances; C_{FGB}, C_{FGS} and C_{FGD} are the parasitic capacitances to bulk, source and drain respectively; and C_T is the sum of all the capacitances connected to the FG ($C_{Gi} \gg C_{FGD}, C_{FGS}, C_{FGB}$):

$$C_T = C_{FGD} + C_{FGS} + C_{FGB} + \sum_{i=1}^{N} C_{Gi} \tag{3}$$

3. BUILDING BLOCKS

The proposed low voltage low power neuron circuit contains two main blocks. These are subthreshold FGMOS current multiplier and sigmoidal circuit (subthreshold FGMOS differential pair) units.

Subthreshold FGMOS Multiplier

Figure 2 shows the four quadrant current multiplier circuit. It is constructed by a one quadrant multiplier (nFG2, nFG4, nFG5 and nFG6) using the translinear principle [3]. Multiplication of the input current is equal to the difference of output current of the circuit [11], output range is not too wide.
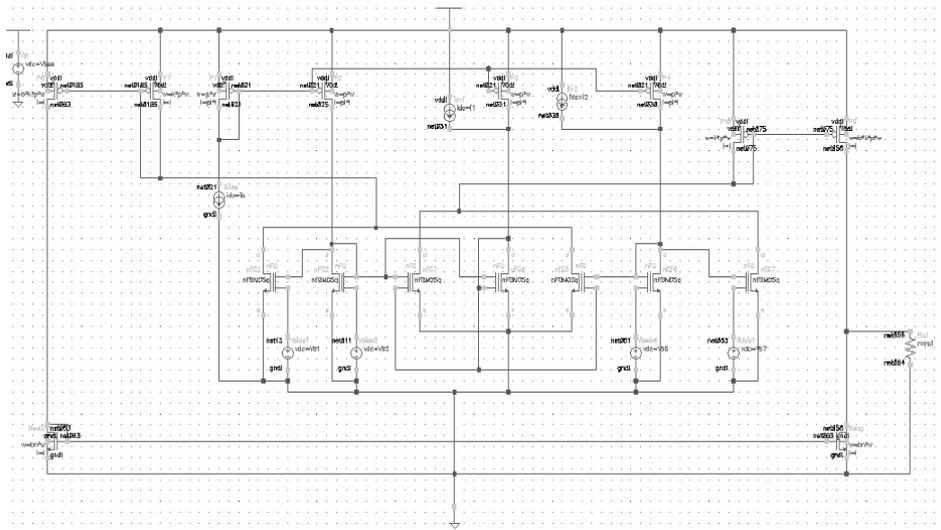

Figure 2. Four-quadrant multiplier

In this study, there is single output current and the output voltage is equal to multiplication of the input current. The output range is rather increased with these improvements: low voltage cascode subthreshold FGMOS current mirrors are used instead of conventional current mirrors and difference of output current is converted to the output voltage. Working principle of the circuit is given below:

$$I_{nFG2} = I_{nFG1} = I_b \tag{4}$$

$$I_{nFG3} = I_{nFG4} = I_{in1} + I_b \tag{5}$$

$$I_{nFG5} = \frac{I_{nFG4} \times I_{nFG6}}{I_{nFG2}} = \frac{(I_{in1}+I_b)(I_{in2}+I_b)}{I_b} \tag{6}$$

$$I_{nFG6} = I_{nFG7} = I_{in2} + I_b \tag{7}$$

If $|I_{in1}|$, $|I_{in2}| < I_b$, then the output currents are given as:

$$I_{OUT1} = I_{nFG1} + I_{nFG5} = I_b + \frac{(I_{in1}+I_b)(I_{in2}+I_b)}{I_b} \tag{8}$$

$$I_{OUT2} = I_{nFG3} + I_{nFG7} = (I_{in1} + I_b) + (I_{in2} + I_b) \tag{9}$$

Output current and voltage are obtained:

$$I_{OUT} = I_{OUT1} - I_{OUT2} = \frac{I_{in1} \times I_{in2}}{I_b} \tag{10}$$

$$V_{OUT} = B.R_{out}.(I_{OUT1} - I_{OUT2}) \tag{11}$$

where B is the reflection ratio of low voltage cascode subthreshold FGMOS current mirrors and maximum value of five should be taken [14].

For our application, we have used 0.35 μm TSMC CMOS process parameters. The supply voltage for the multiplier circuit was 0.75V and simulated using CADENCE simulator.

The dc transfer characteristics of the subthreshold FGMOS multiplier with the input I_{in1} varied -5nA to 5nA and the input I_{in2} taking values from -5nA to 5nA with 2.5nA steps is plotted in Figure 4.
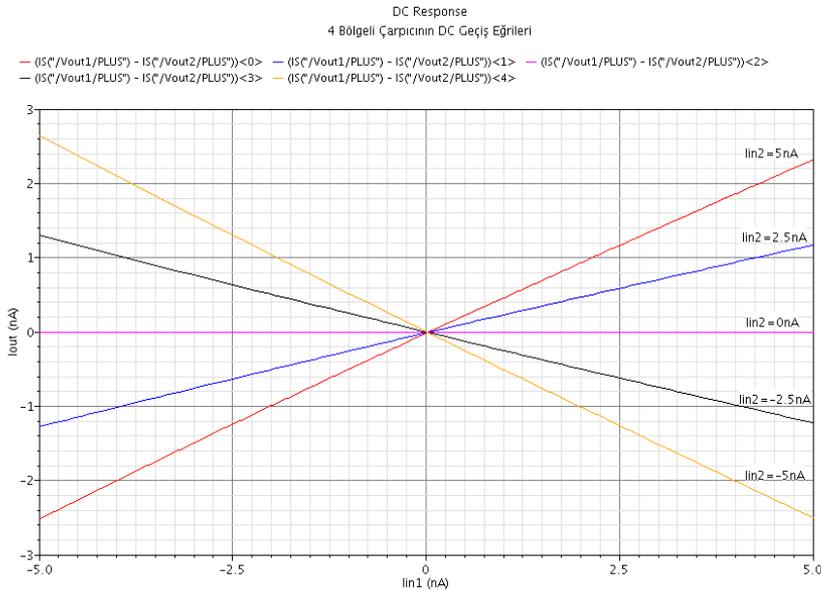

Figure 4. DC transfer characteristics of the multiplier

Sigmoidal Circuit (Subthreshold FGMOS Differential Pair)

By substituting FGMOS transistors instead of input stage MOS transistors in a conventional differential pair, the subthreshold FGMOS differential pair is obtained as in Figure 5. Since FGMOS has a summation of weights, conventional differential pair structure with FGMOS directly realizes sum of multiplication. The output current of the sigmoidal circuit is equal to tangent sigmoid function as seen below.

$$I_0 = I_b tanh \frac{V_{FG1} - V_{FG2}}{2nU_T} \tag{12}$$

where V_{FG1} and V_{FG2} voltages obtained by V_{1+}, V_{2+} and V_{1-}, V_{2-} voltages substituting in Equation 2.
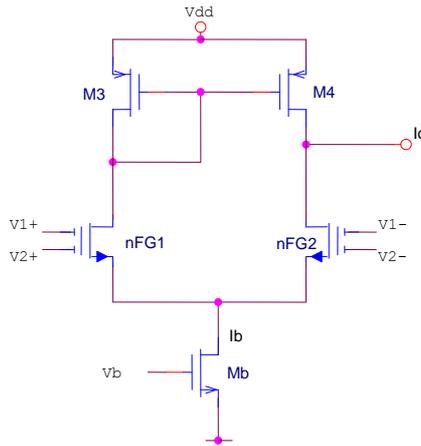

Figure 5. Sigmoidal circuit

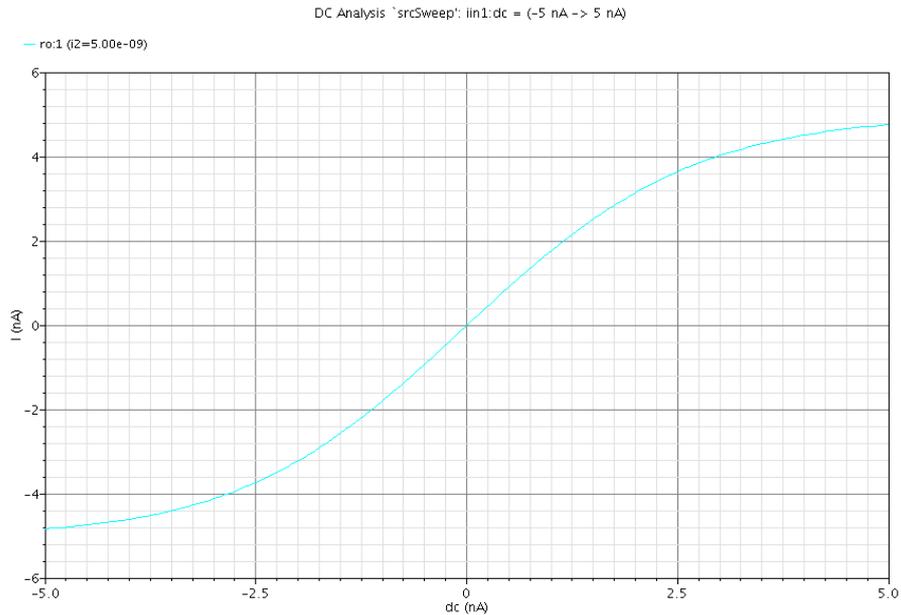The supply voltage for the sigmoidal circuit is 0.5V and dc transfer characteristics is plotted in Figure 6.

DC Analysis `srcSweep`: Iin1:dc = (-5 nA -> 5 nA)

— ro:1 (I2=5.00e-09)

Figure 6. DC transfer characteristics of the sigmoidal circuit

4. THE NEURON CIRCUIT

Simple Neuron Circuit

Neuron circuit block diagram is shown in Figure 7a by the combination of the building blocks neuron is obtained. If we explain this structure shortly, input 'x' is multiplied by its weight 'w' then the sum of these products are applied to an activation function and the output 'y' is obtained. The multiplication, which is mentioned in Figure 7a, is obtained in Figure 7b using a multiplier with two inputs x and w. The summation and the activation function (Figure 7a) are realized by using sigmoidal circuit as shown in Figure 7b.
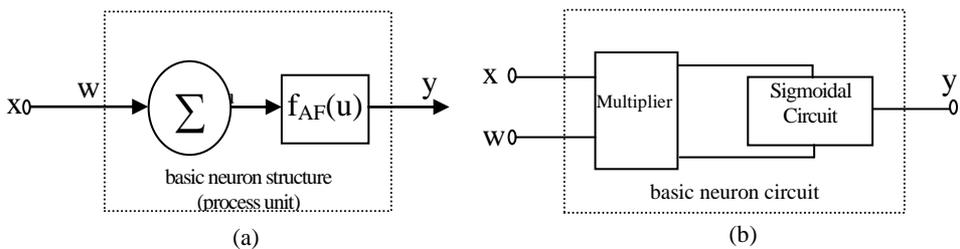
(a)

(b)

Figure 7. (a) Neuron model, (b) Neuron circuit

N-Input Neuron Circuit

N-input neuron circuit shown in Figure 8 can be obtained by generalization of simple neuron circuit. This generalization can also be explained as n-input neuron circuit must have n multipliers, in other words the number of inputs must be equal to the number of multipliers. Multiplier outputs are used as the inputs of subthreshold FGMOS differential pair. As the number of inputs changes the number of multipliers so the input number of subthreshold FGMOS differential pair will change. This change will affect the physical structure of the input stage FGMOS transistors in the differential pair.
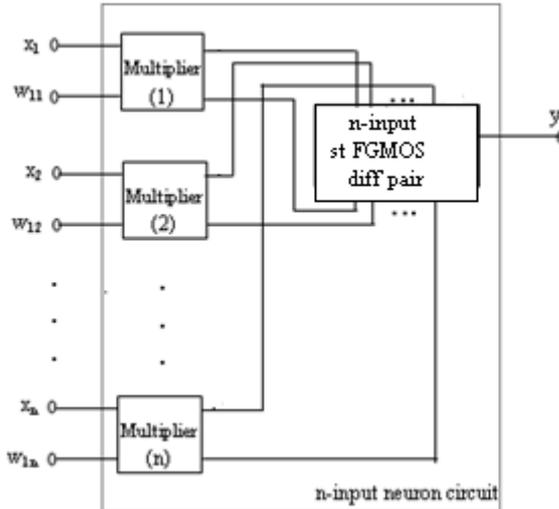

Figure 8. N-input neuron circuit.

5. CONCLUSION

In this work, a modular n-input neuron structure is introduced and applied effectively. ANN structures have been obtained by using these neuron circuits. Simulation results of the low voltage low power neuron circuit proved the efficiency of the proposed neuron circuit. The power consumption required for neuron circuit is 222nW. Low voltage low power subthreshold FGMOS based neuron circuit has single block summation and activation function realization advantage. For complex neural hardware implementations or neural integrated circuit realizations especially to use in pattern recognition field, this neuron block can be used accurately.

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